Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original): A method comprising:

initiating a direct memory access; and

successively transferring data from linked buffers in a first processor system to linked buffers in a second processor system.

Claim 2 (currently amended): The method of claim 1 wherein successively transferring data from linked buffers includes successively transferring data from buffers arranged in a linked list on [[a]] the first processor system to buffers arranged in a linked list on [[a]] the second processor system.

Claim 3 (original): The method of claim 2 including providing descriptors that indicate the status of each of said buffers.

Claim 4 (original): The method of claim 3 including providing flags that indicate whether a buffer is empty or full.

Claim 5 (currently amended): The method of claim 1 including transferring data between buffers within [[in]] a cellular telephone.

Claim 6 (currently amended): The method of claim 5 including transferring data between [[a]] the first processor system that includes a baseband processor and [[a]] the second processor system that includes a multimedia processor of the cellular telephone.

Claim 7 (original): The method of claim 1 including determining the status of a buffer to which data is to be transferred before transferring the data.

Claim 8 (original): The method of claim 7 including determining if a buffer from which data is to be transferred is empty and if so, automatically filling the buffer with data.

Claim 9 (original): The method of claim 8 including generating an interrupt when a buffer is empty and data is to be transferred from the buffer, intercepting the interrupt, and automatically filling the buffer.

Claim 10 (original): The method of claim 9 including determining whether a buffer that is to receive data is full and if the buffer is full, automatically generating an interrupt, intercepting the interrupt, and automatically emptying the buffer.

Claim 11 (original): An article comprising a medium storing instructions that enable a processor-based system to:

initiate a direct memory access; and

successively transfer data from linked buffers in a first processor system to linked buffers in a second processor system.

Claim 12 (currently amended): The article of claim 11 further storing instructions that enable the processor-based system to successively transfer data from linked buffers arranged in a linked list on [[a]] the first processor system to buffers arranged in a linked list on [[a]] the second processor system.

Claim 13 (original): The article of claim 12 further storing instructions that enable the processor-based system to provide descriptors that indicate the status of each of said buffers.

Claim 14 (original): The article of claim 13 further storing instructions that enable the processor-based system to provide flags that indicate whether a buffer is empty or full.

Claim 15 (currently amended): The article of claim 11 further storing instructions that enable the processor-based system to transfer data between buffers within [[in]] a cellular telephone.

Claim 16 (currently amended): The article of claim 15 further storing instructions that enable the processor-based system to transfer data between [[a]] the first processor system that includes a baseband processor and [[a]] the second processor system that includes a multimedia processor of the cellular telephone.

Claim 17 (original): The article of claim 11 further storing instructions that enable the processor-based system to determine the status of a buffer to which data is to be transferred before transferring the data.

Claim 18 (original): The article of claim 17 further storing instructions that enable the processor-based system to determine if a buffer from which data is to be transferred is empty and if so, automatically fill the buffer with data.

Claim 19 (original): The article of claim 18 further storing instructions that enable the processor-based system to generate an interrupt when a buffer is empty and data is to be transferred from the buffer, intercept the interrupt, and automatically fill the buffer.

Claim 20 (original): The article of claim 19 further storing instructions that enable the processor-based system to determine whether a buffer that is to receive data is full and if the buffer is full, automatically generate an interrupt, intercept the interrupt, and automatically empty the buffer.

Claim 21 (original): A system comprising:

a processor; and

a storage coupled to said processor storing instructions that enable the processor to:

initiate a direct memory access; and

successively transfer data from linked buffers in a first processor system to linked buffers in a second processor system.

Claim 22 (currently amended): The system of claim 21 wherein said storage stores instructions that enable the processor to successively transfer data from linked buffers arranged in a linked list on [[a]] the first processor system to buffers arranged in a linked list on [[a]] the second processor system.

Claim 23 (original): The system of claim 22 wherein said storage stores instructions that enable the processor to provide descriptors that indicate the status of each of said buffers.

Claim 24 (original): The system of claim 23 wherein said storage stores instructions that enable the processor to provide flags that indicate whether a buffer is empty or full.

Claim 25 (currently amended): The system of claim 21 wherein said ~~system is~~ linked buffers are within a cellular telephone.

Claim 26 (original): The system of claim 25 wherein said processor is a baseband processor, said system further including a multimedia processor.

Claim 27 (original): The system of claim 21 wherein said storage stores instructions that enable the processor to determine the status of a buffer to which data is to be transferred before transferring the data.

Claim 28 (original): The system of claim 27 wherein said storage stores instructions that enable the processor to determine if a buffer from which data is to be transferred is empty and if so, automatically fill the buffer with data.

Claim 29 (original): The system of claim 28 wherein said storage stores instructions that enable the processor to generate an interrupt when a buffer is empty and data is to be transferred from the buffer, intercept the interrupt, and automatically fill the buffer.

Claim 30 (original): The system of claim 29 wherein said storage stores instructions that enable the processor to determine whether a buffer that is to receive data is full and if the buffer is full, automatically generate an interrupt, intercept the interrupt, and automatically empty the buffer.